WHAT IS CLAIMED IS:

1. A comparator circuit comprising:

a differential amplification circuit including a differential pair transistor for inputting a signal as an object of comparison, and a current mirror load circuit;

a latch circuit including inversion amplifiers that are configured so that an input of one amplifier becomes an input of other amplifier so as to amplify a differential output signal outputted from said current mirror load circuit in accordance with a magnitude relation of said signal as the object of comparison;

an equalization transistor for equalizing a signal of said differential amplification circuit;

a delay circuit for generating a signal to delay a control signal to be inputted in a control electrode of said equalization transistor; and

a control transistor for inputting an output signal of said delay circuit in the control electrode as a control signal to make said latch circuit into an active status and a non-active status.

2. The comparator circuit according to claim 1, wherein said delay circuit comprises an inverter circuit.

3. The comparator circuit according to claim 1, wherein said delay circuit comprises a resister element.

4. A comparator circuit comprising:

a differential amplification circuit including a differential pair transistor for inputting a signal as an object of comparison, and a current mirror load circuit;

a latch circuit including inversion amplifiers that are configured so that an input of one amplifier becomes an input of other amplifier so as to amplify a differential output signal outputted from said current mirror load circuit in accordance with a magnitude relation of said signal as an object of comparison;

an equalization transistor for equalizing a signal of said differential amplification circuit;

a delay circuit for generating a delay control signal to delay a control signal so as to control said equalization transistor;

a logical circuit for outputting a logical multiplication signal of said delay control signal and said control signal as a control signal of said equalization transistor; and

a control transistor for inputting a logical addition signal of said delay control signal and said control signal in the control electrode as a control signal to make said latch circuit into an active status and a non-active status.

5. The comparator circuit according to claim 4, wherein said delay circuit comprises an inverter circuit.

6. The comparator circuit according to claim 4,

wherein said delay circuit comprises a resister element.

7. The comparator circuit according to claim 1, wherein, in said differential amplification circuit, said differential pair includes first conductive transistors (M1, M2) connecting a common-connected source electrode to a constant current source; said current mirror load circuit includes second conductive transistors (M3, M4), which are connected to drain electrodes of said transistors (M1, M2), respectively, and to which drains and gates are connected, and second conductive transistors (M5, M6), of which gates are connected to the gates of said second conductive transistors (M3, M4) with each other; and a comparison result signal is outputted from each drain electrode of said second conductive transistors (M5, M6).

8. The comparator circuit according to claim 4, wherein, in said differential amplification circuit, said differential pair includes first conductive transistors (M1, M2) connecting a common-connected source electrode to a constant current source; said current mirror load circuit includes second conductive transistors (M3, M4), which are connected to drain electrodes of said transistors (M1, M2), respectively, and to which drains and gates are connected, and second conductive transistors (M5, M6), of which gates are connected to the gates of said second conductive transistors (M3, M4) with each other; and a comparison result signal is outputted from each drain

electrode of said second conductive transistors (M5, M6).